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Title: FLASH MEMORY WITH RDRAM INTERFACE

PRELIMINARY  
AMENDMENT

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Commissioner for Patents

Washington, D.C. 20231

IN THE CLAIMS

Please cancel claims 5-13 without prejudice or disclaimer. Please add the following new claims:

14. (New) The flash memory of claim 1, wherein the array of non-volatile memory cells are arranged in a plurality of addressable banks.

15. (New) The flash memory of claim 14, wherein each addressable bank contains addressable sectors of memory cells.

16. (New) The flash memory of claim 1, wherein the output circuitry is adapted to provide the output data starting at a selected location and continuing for a programmed number of locations in a programmed sequence.

17. (New) The flash memory of claim 4, wherein the output circuitry is further adapted to provide the output data starting at a selected location and continuing for a programmed number of locations in a programmed sequence.

18. (New) A flash memory comprising:  
an array of non-volatile memory cells arranged in a plurality of addressable banks;  
data connections;